

**AMENDMENTS TO THE CLAIMS:**

Please amend the Claims as follows:

1. (Currently Amended) A differential amplifier circuit comprising a latch unit and a differential input portion, wherein:

said differential input portion comprises a first transistor and a second transistor each having a first electrode, a second electrode and a control electrode;

the control electrodes of said first and second transistors are supplied with a differential input signal;

a third transistor is inserted between a first power line and a common node to which the first electrodes of said first and second transistors are connected, said third transistor keeps a minute current flowing through said first and second transistors in response to a clock signal at a first level ~~said level~~, said third transistor supplies a first drive current, in response to the clock signal at a second level, said first drive current through said third transistor is larger than said minute current;

a fourth transistor is inserted between said first power line and the common node to which the first electrodes of said first and second transistors are connected, said fourth transistor supplies a second drive current in response to the clock signal at the second level; and

said third transistor is connected in parallel to said fourth transistor.

2. (Canceled)

3. (Previously Presented) The differential amplifier circuit as claimed in claim 1, wherein said third transistor turns off said minute current flowing through said first and second transistors upon deactivation of a power supply to said differential amplifier circuit.

4. (Canceled)

5. (Previously Presented) The differential amplifier circuit as claimed in claim 1, wherein the control electrode of said third transistor is supplied with a first control signal, in response to the clock signal at the first level, for supplying the minute current during the operation of said differential amplifier and a second control signal, in response to the clock signal at the second level, for supplying the first drive current.

6. (Previously Presented) The differential amplifier circuit as claimed in claim 1, wherein a gate width of said third transistor is smaller than a gate width of said fourth transistor.

7. (Canceled)

8. (Previously Presented) The differential amplifier circuit as claimed in claim 1, wherein a first control signal supplied to the control electrode of said third transistor is set to a level for supplying the first drive current at a predetermined level in

response to the clock signal at the second level, while causing the minute current to flow through said first and second transistors in response to the clock signal at the first level during the operation of said differential amplifier.

9. (Original) The differential amplifier circuit as claimed in claim 1, wherein said latch unit comprises:

a first inverter inserted between the second electrode of said first transistor and a second power line; and

a second inverter inserted between the second electrode of said second transistor and said second power line, said first and second inverters being cross-coupled to each other.

10. (Previously Presented) The differential amplifier circuit as claimed in claim 9, wherein:

said differential amplifier circuit is configured of MOS transistors;  
transistors of said first and second inverters which are connected to said second power line are each connected in parallel to an additional transistor, respectively; and  
the second electrode of each of said first and second transistors is held at a predetermined level in response to the clock signal at the first level during the operation of said differential amplifier.

11. (Previously Presented) The differential amplifier circuit as claimed in claim 1, further comprising:

a fifth transistor connected to the second electrode of said first transistor and the second electrode of said second transistor for shorting the second electrodes of said first and second transistors in response to the clock signal at the first level.

12. (Original) The differential amplifier circuit as claimed in claim 1, further comprising:

a sixth transistor connected to the second electrode of said first transistor and the second electrode of said second transistor, said sixth transistor having a control electrode supplied with a predetermined voltage.

13. (Original) The differential amplifier circuit as claimed in claim 12, wherein said differential input signal is at CML level.

14. (Previously Presented) The differential amplifier circuit as claimed in claim 1, further comprising:

a seventh transistor inserted between two nodes for retrieving a differential output signal, said seventh transistor shorting said two nodes in response to the clock signal at the first level.

15. (Previously Presented) The differential amplifier circuit as claimed in claim 1, further comprising:

an eighth transistor inserted between a second power line and the common node to which the first electrodes of said first and second transistors are connected, the control electrode of said eighth transistor being supplied with the clock signal.

16. (Original) The differential amplifier circuit as claimed in claim 1, wherein said differential amplifier circuit is a differential sense amplifier circuit of strong arm latch type.

17. (Currently Amended) A semiconductor integrated circuit device having a differential amplifier circuit receiving a differential signal, a latch circuit latching an output signal of said differential amplifier circuit, and a clock source generating a clock signal and supplying the generated clock signal to said differential amplifier circuit, wherein said differential amplifier circuit comprises a latch unit and a differential input portion, wherein:

said differential input portion comprises a first transistor and a second transistor each having a first electrode, a second electrode and a control electrode;

the control electrodes of said first and second transistors are supplied with the differential input signal;

a third transistor is line and a common node to which the first electrodes of said first and second transistors are connected, inserted between a first power said third

transistor keeps a minute current flowing through said first and second transistors in response to the clock signal at a first level, said third transistor supplies a first drive current, in response to the clock signal at a second level, said drive current through said third transistor is larger than said minute current;

a fourth transistor is inserted between said first power line and the common node to which the first electrodes of said first and second transistors are connected, said fourth transistor supplying a second drive current in response to the clock signal at the second level; and

said third transistor is connected in parallel to said fourth transistor.

18. (Original) The semiconductor integrated circuit device as claimed in claim 17, wherein said semiconductor integrated circuit is a receiving circuit of a signal transmission system, said signal transmission system comprising a transmission circuit outputting the differential signal, a signal transmission path, and said receiving circuit receiving the differential signal through said signal transmission path.

19. (Currently Amended) The semiconductor integrated circuit device as claimed in claim 18, wherein the receiving circuit further comprises:

an equalizer circuit coupled between the transmission circuit and the differential amplifier circuit, wherein the equalizer circuit receives the differential signal, removes an Inter-Symbol Interference of the differential signal by a Partial Response Detection, and

outputs the Inter-Symbol Interference removed differential signal to said differential amplifier circuit.

20. (Currently Amended) A circuit device comprising:

a transmission circuit outputting a differential signal;

a signal transmission path; and

a receiving circuit receiving the differential signal through said signal transmission path, wherein

the receiving circuit comprises a plurality of receiving units, said plurality of receiving units carrying out an interleave operation, and wherein

each of the plurality of receiving units comprises:

a differential amplifier circuit receiving an Inter-Symbol Interference removed differential signal, a latch circuit latching an output signal of said differential amplifier circuit, and a clock source generating a clock signal and supplying the generated clock signal to said differential amplifier circuit, wherein said differential amplifier circuit comprises a latch unit and a differential input portion, wherein:

said differential input portion comprises a first transistor and a second transistor each having a first electrode, a second electrode and a control electrode;

the control electrodes of said first and second transistors are supplied with the Inter-Symbol Interference removed differential input signal;

a third transistor for keeping a minute current to flow through said first and second transistors is inserted between a first power line and a common node to which the

first electrodes of said first and second transistors are connected in response to a first level of the clock signal, wherein said third transistor also supplies a drive current in response to a second level of the clock signal at the time of signal determination in said differential amplifier circuit; and

an equalizer circuit, receiving the differential signal, removing an Inter-Symbol Interference of the differential signal by a Partial Response Detection, and outputting the Inter-Symbol Interference removed differential signal to said differential amplifier circuit.

21. (Canceled)

22. (Previously Presented) The semiconductor integrated circuit device as claimed in claim 17, wherein said third transistor turns off said minute current flowing through said first and second transistors upon deactivation of a power supply to said differential amplifier circuit.

23. (Canceled)

24. (Previously Presented) The semiconductor integrated circuit device as claimed in claim 17, wherein the control electrode of said third transistor is supplied with a first control signal, in response to the clock signal at the first level, for supplying the minute current during the operation of said differential amplifier and a second control

signal, in response to the clock signal at the second level, for supplying the first drive current.

25. (Previously Presented) The semiconductor integrated circuit device as claimed in claim 17, wherein a gate width of said third transistor is smaller than a gate width of said fourth transistor.

26. (Canceled)

27. (Previously Presented) The semiconductor integrated circuit device as claimed in claim 17, wherein a first control signal supplied to the control electrode of said third transistor is set to a level for supplying the first drive current at a predetermined level, in response to the clock signal at the second level, while causing the minute current to flow through said first and second transistors, in response to the clock signal at the first level, during the operation of said differential amplifier.

28. (Original) The semiconductor integrated circuit device as claimed in claim 17, wherein said latch unit comprises:

a first inverter inserted between the second electrode of said first transistor and a second power line; and

a second inverter inserted between the second electrode of said second transistor and said second power line, said first and second inverters being cross-coupled to each other.

29. (Previously Presented) The semiconductor integrated circuit device as claimed in claim 28, wherein:

    said differential amplifier circuit is configured of MOS transistors; transistors of said first and second inverters which are connected to said second power line are each connected in parallel to an additional transistor, respectively; and the second electrode of each of said first and second transistors is held at a predetermined level, in response to the clock signal at the first level, during the operation of said differential amplifier.

30. (Previously Presented) The semiconductor integrated circuit device as claimed in claim 17, wherein said differential amplifier circuit further comprising:

    a fifth transistor connected to the second electrode of said first transistor and the second electrode of said second transistor for shorting the second electrodes of said first and second transistors in response to the clock signal at the first level.

31. (Original) The semiconductor integrated circuit device as claimed in claim 17, wherein said differential amplifier circuit further comprising:

a sixth transistor connected to the second electrode of said first transistor and the second electrode of said second transistor, said sixth transistor having a control electrode supplied with a predetermined voltage.

32. (Original) The semiconductor integrated circuit device as claimed in claim 31, wherein said differential input signal is at CML level.

33. (Currently Amended) The semiconductor integrated circuit device as claimed in claim 17, wherein said differential amplifier circuit further comprising:

a seventh transistor inserted between two nodes for retrieving the ~~a~~ differential output signal of said differential amplifier circuit, said seventh transistor shorting said two nodes in response to the clock signal at the first level.

34. (Previously Presented) The semiconductor integrated circuit device as claimed in claim 17, wherein said differential amplifier circuit further comprising:

an eighth transistor inserted between a second power line and the common node to which the first electrodes of said first and second transistors are connected, the control electrode of said eighth transistor being supplied with the clock signal.

35. (Original) The semiconductor integrated circuit device as claimed in claim 17, wherein said differential amplifier circuit is a differential sense amplifier circuit of strong arm latch type.

36. (Previously Presented) A receiving circuit of a signal transmission system, said signal transmission system comprising a transmission circuit outputting a differential signal, a signal transmission path, and said receiving circuit receiving the differential signal through said signal transmission path, the receiving circuit comprising a receiving unit, wherein the receiving unit comprises:

a differential amplifier circuit, said differential amplifier circuit including a latch unit and a differential input portion, wherein a minute current is kept to flow through said differential input portion;

a latch circuit latching an output signal of said differential amplifier circuit;

a clock source generating a clock and supplying the generated clock to said differential amplifier circuit; and

an equalizer circuit for receiving the differential signal, removing an Inter-Symbol Interference of the differential signal by a Partial Response Detection, and outputting the Inter-Symbol Interference removed differential signal to said differential amplifier circuit.

37. (Previously Presented) The receiving circuit of a signal transmission system as claimed in claim 36, wherein the receiving circuit further comprises at least one additional receiving unit, each additional receiving unit including said differential amplifier circuit, said latch circuit and said equalizer circuit, said receiving circuit carrying out an interleave operation.

38. (Previously Presented) A differential amplifier circuit comprising a latch unit and a differential input portion, wherein:

said differential input portion comprises a first transistor and a second transistor each having a first electrode, a second electrode and a control electrode;

the control electrodes of said first and second transistors are supplied with a differential input signal;

a third transistor is inserted between a first power line and a common node to which the first electrodes of said first and second transistors are connected, a gate electrode of said third transistor receives a control signal of which level is changed in accordance with the operation of said differential amplifier circuit, said third transistor keeps a minute current flowing through said first and second transistors, in response to said control signal at a first level, said third transistor supplies a first drive current, in response to said control signal at a second level, said first drive current through said third transistor is larger than said minute current; and

an eighth transistor inserted between a second power line and the common node to which the first electrodes of said first and second transistors are connected, the control electrode of said eighth transistor being supplied with clock signal.

39. (Previously Presented) A semiconductor integrated circuit device having a differential amplifier circuit receiving a differential signal, a latch circuit latching an output signal of said differential amplifier circuit, and a clock source generating a clock

and supplying the generated clock to said differential amplifier circuit, wherein said differential amplifier circuit comprises a latch unit and a differential input portion, wherein:

said differential input portion comprises a first transistor and a second transistor each having a first electrode, a second electrode and a control electrode;

the control electrodes of said first and second transistors are supplied with the differential input signal;

a third transistor is inserted between a first power line and a common node to which the first electrodes of said first and second transistors are connected, a gate electrode of said third transistor receives a control signal of which level is changed in accordance with the operation of said differential amplifier circuit, said third transistor keeps a minute current flowing through said first and second transistors in response to said control signal at a first level, said third transistor supplies a first drive current in response to said control signal at a second level, said first drive current through said third transistor is larger than said minute current; and

an eighth transistor inserted between a second power line and the common node to which the first electrodes of said first and second transistors are connected, the control electrode of said eighth transistor being supplied with a clock signal.

40. (Canceled)